LITERATURA

[1] KUČERA,L: Kombinatorické algoritmy. SNTL Praha, 1983.

[2] NEUSCHL,Š. a kol.: Modelovanie a simulácia. Alfa/SNTL, 1988.

[3] LIPSETT,R.-MARCHNER,E.-SHAHDAD,M.: VHDL - The Language. IEEE Design & Test, April 1986, s.28-41.

[4] RAZOUK,R.R.: The Use of Petri Nets for Modeling Pipelined Processors. Proc. 25th ACM/IEEE Des.Aut.Conf., Anaheim, 1988, s.548-553.

[5] MEAD,C.A.-CONWAY,L.: Introduction to VLSI Systems. Addison-Vesley, 1980.

[6] MANN.H.: Využití počítače při elektrotechnických návrzích. SNTL/Alfa, 1984.

[7] HAYES,J.P.: An Introduction to Switch-level Modeling. IEEE Design & Test, August 1987, s.18-25.

[8] SZÁNTÓ,L.: Automatizácia projektovania integrovaných obvodov. Alfa, 1985.

[9] BRYANT,R.E. et al: COSMOS: A Compiled Simulator for MOS Circuits.Proc. 24th ACM/IEEE Des.Aut.Conf., Miami, 1987, s.9-15.

[10] WANG.L. et al: SSIM: A Software Levelized Compiled-code Simulator. Proc. 24th ACM/IEEE Des.Aut.Conf., Miami, 1987, s.2-8.

[11] NĚMEC,J.-SOUČEK,J.: Modulární tvorba modelů v simulačním systému ISIS. Návrh obvodů počítačem, Tesla VÚST Praha, 1984, s.9-18.

[12] SMITH,S.P.-MERCER,M.R.-BROCK.B.: Demand Driven Simulation: BACKSIM. Proc. 24th ACM/IEEE Des.Aut.Conf., Miami, 1987, s.181-187.

[13] HWANG,S.Y.-BLANK,T.-CHOI,K.: Incremental Functional Simulation of Digital Circuits. Int.Conf.Computer-Aided Design, 1987, s.392-395.

[14] MILNE,B.: CAE Framework Integrates Multiple Simulators. Electonic Design, vol.37, no.5, 1989, s.77-78.

[15] SLABA,P.:Specializované procesory pro logickou simulaci. Aktuality výpočetní techniky, č.70, 1989, s.80-86.

[16] WALTERS,S.: Reprogrammable Hardware Emulation For ASICs Makes Thorough Design Verification Practical. IEEE Comp. Soc.Int.Conf. COMPCON 89 Spring, 1989, s.484-486.

[17] JAIN,S.K.-AGRAWAL,V.D.: STAFAN: An alternative to fault simulation. Proc. 21st ACM/IEEE Des.Aut.Conf., Albuqurque, 1984, s.18-23.

[18] BRYANT,R.E.: Graph-Based Algorithms for Boolean Function Manipulation. IEEE Transaction on Computers, vol.C-35, no.8, 1986, s.677-691.

[19] MCWILLIAMS,T.M.: Verification of Timing Constraints on Large Digital Systems. Proc. 17th ACM/IEEE Des.Aut.Conf., Minneapolis, 1980, s.139-147.

[20] HITCHCOCK,R.B.: Timing Verification and the Timing Analysis Program. Proc. 19th ACM/IEEE Des.Aut.Conf., Las Vegas, 1982, s.594-604.

[21] SZÁNTÓ,L.: Integrované obvody. Alfa, 1990.

[22] MCFARLAND,M.C.-PARKER,A.C.-CAMPOSAN,R.: Tutorial on High-Level Synthesis. Proc. 25th ACM/IEEE Des.Aut.Conf., Anaheim, 1988, s.330-336.

[23] VLSI Technology. Firemní literatura.

[24] BRAYTON,R.K. et al: Logic Minimization Algorithms for VLSI Synthesis. Hingham, MA:Kluwer Academic Publishers, 1984.

[25] LEHMAN,C.L.: Programmable Logic Design Tools. OrCAD, 1988.

[26] SCHWARZ, J.: Automatizace návrhu kompozice a rozmístění integrovaných obvodů. Kandidátská disertační práce, VUT FE KIVT, Brno, 1983.

[27] BREUER,M.A.editor: Design automation of digital systems. Vol.1. Prentice Hall,1972.
[28] BREUER,M.A.-QUINN,N.R.: A forced directed component placement procedure for printed circuit boards.IEEE Trans. on CAS, vol.26, no. 6, June 1979.
[29] BREUER,M.A.: Min cut placement.J. of design automation and fault tolerant computing,Vol.1,1977.
[30] SCHWARZ,J.:The optimum placement based on a method of limited cuts. Computers and artifficial intelligence, no.5, 1986, s.375-384.
[31] KIRPATRICK,S.-Gelatt,C.D.-Vecchi,M.P.Jr.: Optimization by simulated annealing. Science, vol.220, no.4598, May 1983. package. IEEE J.of SSC, vol.SC-, no.2, 1985.
[33] HOEL,J.H.: Some variations of Lee◂'s algorithm. IEEE Trans. on Computers, vol.C-25, no.1, 1976.
[34] SERVÍT,M.: A new two-phase router. 8th international symposium CAD/CAM, Zagreb, 1986.
[35] TSUKIJAMA,S.-SHIRAKAWA,I.-ASAHARA,S.: An algorithm for the via assigment problem in multilayer backboard wiring. IEEE Trans. on CAS, vol.CAS-26, no.6, 1979.
[36] HONIG,P.: Dvoudimenzionální metody komprese hůlkového diagramu. Návrh obvodů počítačem, Tesla VÚST Praha, 1988, s.216-225.
[37] RIVEST,R.L.-FIDUCCIA,C.M.: A "Greedy" Channel Router. Proc. 19th ACM/IEEE Des.Aut.Conf., Las Vegas, 1982, s.475-481.
[38] LAUTHER,U.: A min-cut placement algorithm for general cell assemblies based on graph representation. Proc. 16th ACM/IEEE Des.Aut.Conf., San Diego, 1979, s.1-10.
[39] MUSIL,L.a kol.: Navrhování mikroelektronických obvodů II. Skriptum VUT, 1991.