

CONTENTS

PREFACE xv

1 INTRODUCTION 1

- 1.1 About Digital Design 1
- 1.2 Analog versus Digital 3
- 1.3 Digital Devices 6
- 1.4 Electronic Aspects of Digital Design 7
- 1.5 Software Aspects of Digital Design 8
- 1.6 Integrated Circuits 11
- 1.7 Programmable Logic Devices 14
- 1.8 Application-Specific ICs 16
- 1.9 Printed-Circuit Boards 17
- 1.10 Digital-Design Levels 18
- 1.11 The Name of the Game 22
- 1.12 Going Forward 23
- Drill Problems 23

2 NUMBER SYSTEMS AND CODES 25

- 2.1 Positional Number Systems 26
- 2.2 Octal and Hexadecimal Numbers 27
- 2.3 General Positional-Number-System Conversions 29
- 2.4 Addition and Subtraction of Nondecimal Numbers 32
- 2.5 Representation of Negative Numbers 34
 - 2.5.1 Signed-Magnitude Representation
 - 2.5.2 Complement Number Systems
 - 2.5.3 Radix-Complement Representation
 - 2.5.4 Two's-Complement Representation
 - 2.5.5 Diminished Radix-Complement Representation
 - 2.5.6 Ones'-Complement Representation
 - 2.5.7 Excess Representations
- 2.6 Two's-Complement Addition and Subtraction 39
 - 2.6.1 Addition Rules
 - 2.6.2 A Graphical View
 - 2.6.3 Overflow
 - 2.6.4 Subtraction Rules
 - 2.6.5 Two's-Complement and Unsigned Binary Numbers
- 2.7 Ones'-Complement Addition and Subtraction 44
- 2.8 Binary Multiplication 45

2.9	Binary Division	47
2.10	Binary Codes for Decimal Numbers	48
2.11	Gray Code	51
2.12	Character Codes	53
2.13	Codes for Actions, Conditions, and States	53
2.14	n -Cubes and Distance	57
2.15	Codes for Detecting and Correcting Errors	58
	2.15.1 Error-Detecting Codes	
	2.15.2 Error-Correcting and Multiple-Error-Detecting Codes	
	2.15.3 Hamming Codes	2.15.4 CRC Codes
	2.15.5 Two-Dimensional Codes	2.15.6 Checksum Codes
	2.15.7 m -out-of- n Codes	
2.16	Codes for Serial Data Transmission and Storage	69
	2.16.1 Parallel and Serial Data	2.16.2 Serial Line Codes
	References	73
	Drill Problems	74
	Exercises	76

3 DIGITAL CIRCUITS 79

3.1	Logic Signals and Gates	80
3.2	Logic Families	84
3.3	CMOS Logic	86
	3.3.1 CMOS Logic Levels	3.3.2 MOS Transistors
	3.3.3 Basic CMOS Inverter Circuit	
	3.3.4 CMOS NAND and NOR Gates	3.3.5 Fan-In
	3.3.6 Noninverting Gates	
	3.3.7 CMOS AND-OR-INVERT and OR-AND-INVERT Gates	
3.4	Electrical Behavior of CMOS Circuits	96
	3.4.1 Overview	3.4.2 Data Sheets and Specifications
3.5	CMOS Static Electrical Behavior	101
	3.5.1 Logic Levels and Noise Margins	
	3.5.2 Circuit Behavior with Resistive Loads	
	3.5.3 Circuit Behavior with Nonideal Inputs	3.5.4 Fanout
	3.5.5 Effects of Loading	3.5.6 Unused Inputs
	3.5.7 How to Destroy a CMOS Device	
3.6	CMOS Dynamic Electrical Behavior	114
	3.6.1 Transition Time	3.6.2 Propagation Delay
	3.6.3 Power Consumption	
	3.6.4 Current Spikes and Decoupling Capacitors	
	3.6.5 Inductive Effects	
	3.6.6 Simultaneous Switching and Ground Bounce	
3.7	Other CMOS Input and Output Structures	129
	3.7.1 Transmission Gates	3.7.2 Schmitt-Trigger Inputs
	3.7.3 Three-State Outputs	3.7.4 Open-Drain Outputs
	3.7.5 Driving LEDs	3.7.6 Multisource Buses
	3.7.7 Wired Logic	
	3.7.8 Pull-Up Resistors	

3.8	CMOS Logic Families	141
3.8.1	<i>HC and HCT</i>	3.8.2 <i>AHC and AHCT</i>
3.8.3	<i>HC, HCT, AHC, and AHCT Electrical Characteristics</i>	
3.8.4	<i>AC and ACT</i>	3.8.5 <i>FCT and FCT-T</i>
3.8.6	<i>FCT-T Electrical Characteristics</i>	
3.9	Low-Voltage CMOS Logic and Interfacing	151
3.9.1	<i>3.3-V LVTTTL and LVC MOS Logic</i>	3.9.2 <i>5-V Tolerant Inputs</i>
3.9.3	<i>5-V Tolerant Outputs</i>	3.9.4 <i>TTL/LVTTTL Interfacing Summary</i>
3.9.5	<i>Logic Levels Less Than 3.3 V</i>	
3.10	Bipolar Logic	155
3.10.1	<i>Diode Logic</i>	3.10.2 <i>Bipolar Junction Transistors</i>
3.10.3	<i>Transistor-Transistor Logic</i>	
3.10.4	<i>TTL Logic Levels and Noise Margins</i>	3.10.5 <i>TTL Fanout</i>
3.10.6	<i>TTL Families</i>	3.10.7 <i>A TTL Data Sheet</i>
3.10.8	<i>CMOS/TTL Interfacing</i>	3.10.9 <i>Emitter-Coupled Logic</i>
	References	174
	Drill Problems	175
	Exercises	179
4	COMBINATIONAL LOGIC DESIGN PRINCIPLES	183
4.1	Switching Algebra	184
4.1.1	<i>Axioms</i>	4.1.2 <i>Single-Variable Theorems</i>
4.1.3	<i>Two- and Three-Variable Theorems</i>	
4.1.4	<i>n-Variable Theorems</i>	4.1.5 <i>Duality</i>
4.1.6	<i>Standard Representations of Logic Functions</i>	
4.2	Combinational-Circuit Analysis	199
4.3	Combinational-Circuit Synthesis	205
4.3.1	<i>Circuit Descriptions and Designs</i>	4.3.2 <i>Circuit Manipulations</i>
4.3.3	<i>Combinational-Circuit Minimization</i>	4.3.4 <i>Karnaugh Maps</i>
4.3.5	<i>Minimizing Sums of Products</i>	4.3.6 <i>Other Minimization Topics</i>
4.3.7	<i>Programmed Minimization Methods</i>	
4.4	Timing Hazards	224
4.4.1	<i>Static Hazards</i>	4.4.2 <i>Finding Static Hazards Using Maps</i>
4.4.3	<i>Dynamic Hazards</i>	4.4.4 <i>Designing Hazard-Free Circuits</i>
	References	229
	Drill Problems	230
	Exercises	232
5	HARDWARE DESCRIPTION LANGUAGES	237
5.1	HDL-Based Digital Design	238
5.1.1	<i>Why HDLs?</i>	5.1.2 <i>HDL Tool Suites</i>
5.1.3	<i>HDL-Based Design Flow</i>	
5.2	The ABEL Hardware Description Language	243
5.2.1	<i>ABEL Program Structure</i>	5.2.2 <i>ABEL Compiler Operation</i>
5.2.3	<i>WHEN Statements and Equation Blocks</i>	5.2.4 <i>Truth Tables</i>
5.2.5	<i>Ranges, Sets, and Relations</i>	5.2.6 <i>Test Vectors</i>
5.2.7	<i>Additional ABEL Features</i>	

5.3	The VHDL Hardware Description Language	256
5.3.1	Program Structure	
5.3.2	Types, Constants, and Arrays	
5.3.3	Functions and Procedures	
5.3.4	Libraries and Packages	
5.3.5	Structural Design Elements	
5.3.6	Dataflow Design Elements	
5.3.7	Behavioral Design Elements	
5.3.8	The Time Dimension	
5.3.9	Simulation	
5.3.10	Test Benches	
5.3.11	VHDL Features for Sequential Logic Design	
5.3.12	Synthesis	
5.4	The Verilog Hardware Description Language	290
5.4.1	Program Structure	
5.4.2	Logic System, Nets, Variables, and Constants	
5.4.3	Vectors and Operators	
5.4.4	Arrays	
5.4.5	Logical Operators and Expressions	
5.4.6	Compiler Directives	
5.4.7	Structural Design Elements	
5.4.8	Dataflow Design Elements	
5.4.9	Behavioral Design Elements (Procedural Code)	
5.4.10	Functions and Tasks	
5.4.11	The Time Dimension	
5.4.12	Simulation	
5.4.13	Test Benches	
5.4.14	Verilog Features for Sequential Logic Design	
5.4.15	Synthesis	
	References	335
	Drill Problems	337
	Exercises	338

6 COMBINATIONAL LOGIC DESIGN PRACTICES 341

6.1	Documentation Standards	342
6.1.1	Block Diagrams	
6.1.2	Gate Symbols	
6.1.3	Signal Names and Active Levels	
6.1.4	Active Levels for Pins	
6.1.5	Bubble-to-Bubble Logic Design	
6.1.6	Signal Naming in HDL Programs	
6.1.7	Drawing Layout	
6.1.8	Buses	
6.1.9	Additional Schematic Information	
6.2	Circuit Timing	362
6.2.1	Timing Diagrams	
6.2.2	Propagation Delay	
6.2.3	Timing Specifications	
6.2.4	Timing Analysis	
6.2.5	Timing Analysis Tools	
6.3	Combinational PLDs	370
6.3.1	Programmable Logic Arrays	
6.3.2	Programmable Array Logic Devices	
6.3.3	Generic Array Logic Devices	
6.3.4	Complex Programmable Logic Devices (CPLDs)	
6.3.5	CMOS PLD Circuits	
6.3.6	Device Programming and Testing	
6.4	Decoders	384
6.4.1	Binary Decoders	
6.4.2	Logic Symbols for Larger-Scale Elements	
6.4.3	The 74x138 3-to-8 Decoder	
6.4.4	Cascading Binary Decoders	
6.4.5	Decoders in ABEL and PLDs	
6.4.6	Decoders in VHDL	
6.4.7	Decoders in Verilog	
6.4.8	Seven-Segment Decoders	
6.5	Encoders	408
6.5.1	Priority Encoders	
6.5.2	The 74x148 Priority Encoder	
6.5.3	Encoders in ABEL and PLDs	
6.5.4	Encoders in VHDL	
6.5.5	Encoders in Verilog	

6.6	Three-State Devices	418
6.6.1	Three-State Buffers	6.6.2 Standard MSI Three-State Buffers
6.6.3	Three-State Outputs in ABEL and PLDs	
6.6.4	Three-State Outputs in VHDL	
6.6.5	Three-State Outputs in Verilog	
6.7	Multiplexers	432
6.7.1	Standard MSI Multiplexers	6.7.2 Expanding Multiplexers
6.7.3	Multiplexers, Demultiplexers, and Buses	
6.7.4	Multiplexers in ABEL and PLDs	6.7.5 Multiplexers in VHDL
6.7.6	Multiplexers in Verilog	
6.8	Exclusive-OR Gates and Parity Circuits	447
6.8.1	Exclusive-OR and Exclusive-NOR Gates	6.8.2 Parity Circuits
6.8.3	The 74x280 9-Bit Parity Generator	
6.8.4	Parity-Checking Applications	
6.8.5	Exclusive-OR Gates and Parity Circuits in ABEL and PLDs	
6.8.6	Exclusive-OR Gates and Parity Circuits in VHDL	
6.8.7	Exclusive-OR Gates and Parity Circuits in Verilog	
6.9	Comparators	458
6.9.1	Comparator Structure	6.9.2 Iterative Circuits
6.9.3	An Iterative Comparator Circuit	
6.9.4	Standard MSI Magnitude Comparators	
6.9.5	Comparators in HDLs	6.9.6 Comparators in ABEL and PLDs
6.9.7	Comparators in VHDL	6.9.8 Comparators in Verilog
6.10	Adders, Subtractors, and ALUs	474
6.10.1	Half Adders and Full Adders	6.10.2 Ripple Adders
6.10.3	Subtractors	6.10.4 Carry-Lookahead Adders
6.10.5	MSI Adders	6.10.6 MSI Arithmetic and Logic Units
6.10.7	Group-Carry Lookahead	6.10.8 Adders in ABEL and PLDs
6.10.9	Adders in VHDL	6.10.10 Adders in Verilog
6.11	Combinational Multipliers	494
6.11.1	Combinational Multiplier Structures	
6.11.2	Multiplication in ABEL and PLDs	6.11.3 Multiplication in VHDL
6.11.4	Multiplication in Verilog	
	References	508
	Drill Problems	509
	Exercises	511

7 SEQUENTIAL LOGIC DESIGN PRINCIPLES 521

7.1	Bistable Elements	523
7.1.1	Digital Analysis	7.1.2 Analog Analysis
7.1.3	Metastable Behavior	
7.2	Latches and Flip-Flops	526
7.2.1	S-R Latch	7.2.2 $\bar{S}\text{-}\bar{R}$ Latch
7.2.3	S-R Latch with Enable	
7.2.4	D Latch	7.2.5 Edge-Triggered D Flip-Flop
7.2.6	Edge-Triggered D Flip-Flop with Enable	7.2.7 Scan Flip-Flop
7.2.8	Master/Slave S-R Flip-Flop	7.2.9 Master/Slave J-K Flip-Flop
7.2.10	Edge-Triggered J-K Flip-Flop	7.2.11 T Flip-Flop

7.3	Clocked Synchronous State-Machine Analysis	542
7.3.1	<i>State-Machine Structure</i>	
7.3.2	<i>Output Logic</i>	
7.3.3	<i>Characteristic Equations</i>	
7.3.4	<i>Analysis of State Machines with D Flip-Flops</i>	
7.4	Clocked Synchronous State-Machine Design	553
7.4.1	<i>State-Table Design Example</i>	
7.4.2	<i>State Minimization</i>	
7.4.3	<i>State Assignment</i>	
7.4.4	<i>Synthesis Using D Flip-Flops</i>	
7.4.5	<i>Synthesis Using J-K Flip-Flops</i>	
7.4.6	<i>More Design Examples Using D Flip-Flops</i>	
7.5	Designing State Machines Using State Diagrams	570
7.6	State-Machine Synthesis Using Transition Lists	577
7.6.1	<i>Transition Equations</i>	
7.6.2	<i>Excitation Equations</i>	
7.6.3	<i>Variations on the Scheme</i>	
7.6.4	<i>Realizing the State Machine</i>	
7.7	Another State-Machine Design Example	580
7.7.1	<i>The Guessing Game</i>	
7.7.2	<i>Unused States</i>	
7.7.3	<i>Output-Coded State Assignment</i>	
7.7.4	<i>“Don’t-Care” State Codings</i>	
7.8	Decomposing State Machines	587
7.9	Feedback Sequential-Circuit Analysis	590
7.9.1	<i>Basic Analysis</i>	
7.9.2	<i>Analyzing Circuits with Multiple Feedback Loops</i>	
7.9.3	<i>Races</i>	
7.9.4	<i>State Tables and Flow Tables</i>	
7.9.5	<i>CMOS D Flip-Flop Analysis</i>	
7.10	Feedback Sequential-Circuit Design	601
7.10.1	<i>Latches</i>	
7.10.2	<i>Designing Fundamental-Mode Flow Table</i>	
7.10.3	<i>Flow-Table Minimization</i>	
7.10.4	<i>Race-Free State Assignment</i>	
7.10.5	<i>Excitation Equations</i>	
7.10.6	<i>Essential Hazards</i>	
7.10.7	<i>Summary</i>	
7.11	ABEL Sequential-Circuit Design Features	612
7.11.1	<i>Registered Outputs</i>	
7.11.2	<i>State Diagrams</i>	
7.11.3	<i>External State Memory</i>	
7.11.4	<i>Specifying Moore Outputs</i>	
7.11.5	<i>Specifying Mealy and Pipelined Outputs with WITH</i>	
7.11.6	<i>Test Vectors</i>	
7.12	Sequential-Circuit Design with VHDL	625
7.12.1	<i>Clocked Circuits</i>	
7.12.2	<i>State-Machine Design with VHDL</i>	
7.12.3	<i>A VHDL State-Machine Example</i>	
7.12.4	<i>State Assignment in VHDL</i>	
7.12.5	<i>Pipelined Outputs in VHDL</i>	
7.12.6	<i>Direct VHDL Coding Without a State Table</i>	
7.12.7	<i>More VHDL State-Machine Examples</i>	
7.12.8	<i>Specifying Flip-Flops in VHDL</i>	
7.12.9	<i>VHDL State-Machine Test Benches</i>	
7.12.10	<i>Feedback Sequential Circuits</i>	
7.13	Sequential-Circuit Design with Verilog	646
7.13.1	<i>Clocked Circuits</i>	
7.13.2	<i>State-Machine Design with Verilog</i>	
7.13.3	<i>A Verilog State-Machine Example</i>	
7.13.4	<i>Pipelined Outputs in Verilog</i>	
7.13.5	<i>Direct Verilog Coding Without a State Table</i>	
7.13.6	<i>More Verilog State-Machine Examples</i>	

- 7.13.7 *Specifying Flip-Flops in Verilog*
- 7.13.8 *Verilog State-Machine Test Benches*
- 7.13.9 *Feedback Sequential Circuits*

References 663

Drill Problems 664

Exercises 669

8 SEQUENTIAL LOGIC DESIGN PRACTICES 679

8.1 Sequential-Circuit Documentation Standards 680

- 8.1.1 *General Requirements*
- 8.1.2 *Logic Symbols*
- 8.1.3 *State-Machine Descriptions*
- 8.1.4 *Timing Diagrams and Specifications*

8.2 Latches and Flip-Flops 686

- 8.2.1 *SSI Latches and Flip-Flops*
- 8.2.2 *Switch Debouncing*
- 8.2.3 *The Simplest Switch Debouncer*
- 8.2.4 *Bus Holder Circuit*
- 8.2.5 *Multibit Registers and Latches*
- 8.2.6 *Registers and Latches in ABEL and PLDs*
- 8.2.7 *Registers and Latches in VHDL*
- 8.2.8 *Registers and Latches in Verilog*

8.3 Sequential PLDs 703

- 8.3.1 *Sequential GAL Devices*
- 8.3.2 *PLD Timing Specifications*

8.4 Counters 710

- 8.4.1 *Ripple Counters*
- 8.4.2 *Synchronous Counters*
- 8.4.3 *MSI Counters and Applications*
- 8.4.4 *Decoding Binary-Counter States*
- 8.4.5 *Counters in ABEL and PLDs*
- 8.4.6 *Counters in VHDL*
- 8.4.7 *Counters in Verilog*

8.5 Shift Registers 727

- 8.5.1 *Shift-Register Structure*
- 8.5.2 *MSI Shift Registers*
- 8.5.3 *Shift-Register Counters*
- 8.5.4 *Ring Counters*
- 8.5.5 *Johnson Counters*
- 8.5.6 *Linear Feedback Shift-Register Counters*
- 8.5.7 *Shift Registers in ABEL and PLDs*
- 8.5.8 *Shift Registers in VHDL*
- 8.5.9 *Shift Registers in Verilog*

8.6 Iterative versus Sequential Circuits 756

8.7 Synchronous Design Methodology 758

- 8.7.1 *Synchronous System Structure*

8.8 Impediments to Synchronous Design 762

- 8.8.1 *Clock Skew*
- 8.8.2 *Gating the Clock*
- 8.8.3 *Asynchronous Inputs*

8.9 Synchronizer Failure and Metastability 769

- 8.9.1 *Synchronizer Failure*
- 8.9.2 *Metastability Resolution Time*
- 8.9.3 *Reliable Synchronizer Design*
- 8.9.4 *Analysis of Metastable Timing*
- 8.9.5 *Better Synchronizers*
- 8.9.6 *Other Synchronizer Designs*
- 8.9.7 *Synchronizing High-Speed Data Transfers*

References 788

Drill Problems 790

Exercises 792

9	MEMORY, CPLDS, AND FPGAS	799
9.1	Read-Only Memory	800
9.1.1	Using ROMs for “Random” Combinational Logic Functions	
9.1.2	Internal ROM Structure	9.1.3 Two-Dimensional Decoding
9.1.4	Commercial ROM Types	
9.1.5	ROM Control Inputs and Timing	9.1.6 ROM Applications
9.2	Read/Write Memory	821
9.3	Static RAM	822
9.3.1	Static-RAM Inputs and Outputs	
9.3.2	Static-RAM Internal Structure	
9.3.3	Static-RAM Timing	9.3.4 Standard Static RAMs
9.3.5	Synchronous SRAM	
9.4	Dynamic RAM	833
9.4.1	Dynamic-RAM Structure	9.4.2 SDRAM Timing
9.4.3	DDR SDRAMs	
9.5	Complex Programmable Logic Devices	840
9.5.1	Xilinx XC9500 CPLD Family	
9.5.2	Function-Block Architecture	
9.5.3	Input/Output-Block Architecture	9.5.4 Switch Matrix
9.6	Field-Programmable Gate Arrays	850
9.6.1	Xilinx XC4000 FPGA Family	9.6.2 Configurable Logic Block
9.6.3	Input/Output Block	9.6.4 Programmable Interconnect
	References	859
	Drill Problems	859
	Exercises	860
INDEX	863	