

CONTENTS

ABOUT AUTHOR	4
1 INTRODUCTION.....	5
2 PRINCIPLES OF WIRELESS DIGITAL COMMUNICATION.....	5
2.1 Generalized model of communication system.....	7
2.2 Data detection	7
3 JOINT PHASE AND TIMING SYNCHRONIZER	9
4 ERROR DETECTORS IN SYNCHRONIZERS	11
4.1 Phase error detectors.....	11
4.2 Timing error detectors.....	16
5 DIGITAL LOCKED LOOPS FOR SYNCHRONIZERS	18
5.1 Derivation of 1 st order DPLL based on analog template	19
5.2 2 nd order DPLL.....	21
5.3 Equivalent model of digital locked loop.....	21
5.4 Equivalent model of JPT synchronizer	24
6 SDR DEMODULATOR BASED ON JPT ESTIMATOR	26
7 CONCLUSIONS.....	27
REFERENCES.....	28
ABSTRAKT.....	31