## CONTENTS

Web Site for Computer Organization and Architecture, Sixth Edition vi Preface xv About the Author xxi

### PART ONE OVERVIEW 1

#### CHAPTER 1 Introduction 3

- 1.1 Organization and Architecture 4
- 1.2 Structure and Function 5
- 1.3 Why Study Computer Organization and Architecture? 10
- 1.4 Outline of the Book 13
- 1.5 Internet and Web Resources 13

## CHAPTER 2 Computer Evolution and Performance 15

- 2.1 A Brief History of Computers 16
- 2.2 Designing for Performance 37
- 2.3 Pentium and PowerPC Evolution 41
- 2.4 Recommended Reading and Web Sites 44
- 2.5 Key Terms, Review Questions, and Problems 45

## PART TWO THE COMPUTER SYSTEM 47

# CHAPTER 3 A Top-Level View of Computer Function and Interconnection 49

- 3.1 Computer Components 50
- 3.2 Computer Function 53
- 3.3 Interconnection Structures 67
- 3.4 Bus Interconnection 69
- 3.5 PCI 79
- 3.6 Recommended Reading and Web Sites 89
- 3.7 Key Terms, Review Questions, and Problems 90 Appendix 3A: Timing Diagrams 92

## CHAPTER 4 Cache Memory 95

- 4.1 Computer Memory System Overview 96
- 4.2 Cache Memory Principles 103
- 4.3 Elements of Cache Design 106
- 4.4 Pentium 4 and PowerPC Cache Organizations 121
- 4.5 Recommended Reading 125
- 4.6 Key Terms, Review Questions, and Problems 125

Appendix 4A: Performance Characteristics of

Two-Level Memories 128

## CHAPTER 5 Internal Memory 137

- 5.1 Semiconductor Main Memory 138
- 5.2 Error Correction 148
- 5.3 Advanced DRAM Organization 154
- 5.4 Recommended Reading and Web Sites 159
- 5.5 Key Terms, Review Questions, and Problems 160

### **CHAPTER 6 External Memory 163**

- 6.1 Magnetic Disk 164
- 6.2 RAID 174
- 6.3 Optical Memory 184
- 6.4 Magnetic Tape 189
- 6.5 Recommended Reading and Web Sites 191
- 6.6 Key Terms, Review Questions, and Problems 192

### CHAPTER 7 Input/Output 195

- 7.1 External Devices 197
- 7.2 I/O Modules 201
- 7.3 Programmed I/O 204
- 7.4 Interrupt-Driven I/O 208
- 7.5 Direct Memory Access 216
- 7.6 I/O Channels and Processors 220
- 7.7 The External Interface: FireWire and InfiniBand 223
- 7.8 Recommended Reading and Web Sites 233
- 7.9 Key Terms, Review Questions, and Problems 233

## **CHAPTER 8 Operating System Support 237**

- 8.1 Operating System Overview 238
- 8.2 Scheduling 250
- 8.3 Memory Management 256
- 8.4 Pentium II and PowerPC Memory Management 269
- 8.5 Recommended Reading and Web Sites 277
- 8.6 Key Terms, Review Questions, and Problems 278

# PART THREE THE CENTRAL PROCESSING UNIT 281

## CHAPTER 9 Computer Arithmetic 283

- 9.1 The Arithmetic and Logic Unit 284
- 9.2 Integer Representation 285
- 9.3 Integer Arithmetic 291
- 9.4 Floating-Point Representation 307
- 9.5 Floating-Point Arithmetic 313
- 9.6 Recommended Reading and Web Sites 324
- 9.7 Key Terms, Review Questions, and Problems 325

#### CHAPTER 10 Instruction Sets: Characteristics and Functions 329

- 10.1 Machine Instruction Characteristics 330
- 10.2 Types of Operands 337
- 10.3 Pentium and PowerPC Data Types 339
- 10.4 Types of Operations 341
- 10.5 Pentium and PowerPC Operation Types 355
- 10.6 Assembly Language 364
- 10.7 Recommended Reading 366
  - 10.8 Key Terms, Review Questions, and Problems 367

Appendix 10A: Stacks 371

Appendix 10B: Little-, Big-, and Bi-Endian 376

# CHAPTER 11 Instruction Sets: Addressing Modes and Formats 381

- 11.1 Addressing 382
- 11.2 Pentium and PowerPC Addressing Modes 389
  - 11.3 Instruction Formats 395
  - 11.4 Pentium and PowerPC Instruction Formats 404
    - 11.5 Recommended Reading 408
    - 11.6 Key Terms, Review Questions, and Problems 409

### CHAPTER 12 CPU Structure and Function 411

- 12.1 Processor Organization 412
- 12.2 Register Organization 414
  - 12.3 Instruction Cycle 420
  - 12.4 Instruction Pipelining 424
  - 12.5 The Pentium Processor 440
  - 12.6 The PowerPC Processor 450
  - 12.7 Recommended Reading 457
  - 12.8 Key Terms, Review Questions, and Problems 458

## CHAPTER 13 Reduced Instruction Set Computers 461

- 13.1 Instruction Execution Characteristics 463
- 13.2 The Use of a Large Register File 467
  - 13.3 Compiler-Based Register Optimization 473
  - 13.4 Reduced Instruction Set Architecture 474
  - 13.5 RISC Pipelining 482
    - 13.6 MIPS R4000 486
- 13.7 SPARC 494
  - 13.8 RISC versus CISC Controversy 500
  - 13.9 Recommended Reading 501
  - 13.10 Key Terms, Review Questions, and Problems 502

## CHAPTER 14 Instruction-Level Parallelism and Superscalar Processors 505

- 14.1 Overview 507
- 14.2 Design Issues 511
- 14.3 Pentium 4 520
- 14.4 PowerPC 527
- 14.5 Recommended Reading 535
- 14.6 Key Terms, Review Questions, and Problems 536

#### CHAPTER 15 The IA-64 Architecture 541

- 15.1 Motivation 543
- 15.2 General Organization 544
- 15.3 Predication, Speculation, and Software Pipelining 546
- 15.4 IA-64 Instruction Set Architecture 563
- 15.5 Itanium Organization 568
- 15.6 Recommended Reading and Web Sites 569
- 15.7 Key Terms, Review Questions, and Problems 570

#### PART FOUR THE CONTROL UNIT 573

### CHAPTER 16 Control Unit Operation 575

- 16.1 Micro-Operations 577
- 16.2 Control of the Processor 583
- 16.3 Hardwired Implementation 594
- 16.4 Recommended Reading 597
- 16.5 Key Terms, Review Questions, and Problems 597

## CHAPTER 17 Microprogrammed Control 599

- 17.1 Basic Concepts 600
- 17.2 Microinstruction Sequencing 609
- 17.3 Microinstruction Execution 615
- 17.4 TI 8800 627
- 17.5 Applications of Microprogramming 637
- 17.6 Recommended Reading 638
- 17.7 Key Terms, Review Questions, and Problems 639

## PART FIVE PARALLEL ORGANIZATION 641

## CHAPTER 18 Parallel Processing 643

- 18.1 Multiple Processor Organizations 645
- 18.2 Symmetric Multiprocessors 647
- 18.3 Cache Coherence and the MESI Protocol 656
- 18.4 Clusters 663
- 18.5 Nonuniform Memory Access 670
- 18.6 Vector Computation 674
- 18.7 Recommended Reading 687
- 18.8 Key Terms, Review Questions, and Problems 688

#### **APPENDICES**

### APPENDIX A Digital Logic 693

- A.1 Boolean Algebra 694
- A.2 Gates 696
- A.3 Combinational Circuits 699
- A.4 Sequential Circuits 720
- A.5 Problems 730

### APPENDIX B Number Systems 733

- B.1 The Decimal System 734
- B.2 The Binary System 734
- B.3 Converting between Binary and Decimal 735
- B.4 Hexadecimal Notation 738
- B.5 Problems 739

# APPENDIX C Projects for Teaching Computer Organization and Architecture 741

- C.1 Research Projects 742
- C.2 Simulation Projects 742
- C.3 Reading/Report Assignments 743

**GLOSSARY 745** 

**REFERENCES 757** 

INDEX 773