

Contents

CHAPTER 1 Introduction

1.1	A Brief History	1
1.2	Book Summary	5
1.3	MOS Transistors	7
1.4	CMOS Logic	10
1.4.1	The Inverter 10	
1.4.2	The NAND Gate 10	
1.4.3	Combinational Logic 11	
1.4.4	The NOR Gate 12	
1.4.5	Compound Gates 13	
1.4.6	Pass Transistors and Transmission Gates 14	
1.4.7	Tristates 17	
1.4.8	Multiplexers 18	
1.4.9	Latches and Flip-Flops 20	
1.5	CMOS Fabrication and Layout	23
1.5.1	Inverter Cross-section 23	
1.5.2	Fabrication Process 24	
1.5.3	Layout Design Rules 28	
1.5.4	Gate Layout 32	
1.5.5	Stick Diagrams 33	
1.6	Design Partitioning	35
1.7	Example: A Simple MIPS Microprocessor	39
1.7.1	MIPS Architecture 39	
1.7.2	Multicycle MIPS Microarchitecture 42	
1.8	Logic Design	46
1.8.1	Top-level Interface 46	
1.8.2	Block Diagram 47	
1.8.3	Hierarchy 47	
1.8.4	Hardware Description Languages 48	
1.9	Circuit Design	49
1.10	Physical Design	52

1.10.1	Floorplanning	52
1.10.2	Standard Cells	55
1.10.3	Snap-together Cells	55
1.10.4	Slice Plans	59
1.10.5	Area Estimation	59
1.11	Design Verification	60
1.12	Fabrication, Packaging, and Testing	61
	Summary	63
	Exercises	63

CHAPTER 2 MOS Transistor Theory

2.1	Introduction	67
2.2	Ideal I-V Characteristics	71
2.3	C-V Characteristics	75
2.3.1	Simple MOS Capacitance Models	75
2.3.2	Detailed MOS Gate Capacitance Model	77
2.3.3	Detailed MOS Diffusion Capacitance Model	80
2.4	Nonideal I-V Effects	83
2.4.1	Velocity Saturation and Mobility Degradation	84
2.4.2	Channel Length Modulation	86
2.4.3	Body Effect	87
2.4.4	Subthreshold Conduction	88
2.4.5	Junction Leakage	89
2.4.6	Tunneling	90
2.4.7	Temperature Dependence	90
2.4.8	Geometry Dependence	92
2.4.9	Summary	92
2.5	DC Transfer Characteristics	94
2.5.1	Complementary CMOS Inverter DC Characteristics	94
2.5.2	Beta Ratio Effects	97
2.5.3	Noise Margin	98
2.5.4	Ratioed Inverter Transfer Function	100
2.5.5	Pass Transistor DC Characteristics	101
2.5.6	Tristate Inverter	102
2.6	Switch-level RC Delay Models	103
2.7	Pitfalls and Fallacies	106
	Summary	107
	Exercises	108

CHAPTER 3 CMOS Processing Technology

3.1	Introduction	113
3.2	CMOS Technologies	113
3.2.1	Background	113
3.2.2	Wafer Formation	114
3.2.3	Photolithography	115
3.2.4	Well and Channel Formation	117
3.2.5	Silicon Dioxide (SiO ₂)	118
3.2.6	Isolation	119
3.2.7	Gate Oxide	120
3.2.8	Gate and Source/Drain Formation	121
3.2.9	Contacts and Metallization	124
3.2.10	Passivation	124
3.2.11	Metrology	125
3.3	Layout Design Rules	125
3.3.1	Design Rule Background	126
3.3.2	Scribe Line and Other Structures	130
3.3.3	MOSIS Scalable CMOS Design Rules	130
3.3.4	Micron Design Rules	134
3.4	CMOS Process Enhancements	136
3.4.1	Transistors	136
3.4.2	Interconnect	140
3.4.3	Circuit Elements	141
3.4.4	Beyond Conventional CMOS	148
3.5	Technology-related CAD Issues	148
3.5.1	Design Rule Checking (DRC)	149
3.5.2	Circuit Extraction	150
3.6	Manufacturing Issues	151
3.6.1	Antenna Rules	151
3.6.2	Layer Density Rules	152
3.6.3	Resolution Enhancement Rules	153
3.7	Pitfalls and Fallacies	153
3.8	Historical Perspective	154
	Summary	154
	Exercises	154

CHAPTER 4 Circuit Characterization and Performance Estimation

4.1	Introduction	157
4.2	Delay Estimation	158
4.2.1	RC Delay Models	159
4.2.2	Linear Delay Model	165
4.2.3	Logical Effort	166
4.2.4	Parasitic Delay	167
 4.2.5	Limitations to the Linear Delay Model	169
4.3	Logical Effort and Transistor Sizing	173
4.3.1	Delay in a Logic Gate	173
4.3.2	Delay in Multistage Logic Networks	174
4.3.3	Choosing the Best Number of Stages	178
4.3.4	Example	181
4.3.5	Summary and Observations	183
 4.3.6	Limitations of Logical Effort	185
 4.3.7	Extracting Logical Effort from Datasheets	185
4.4	Power Dissipation	186
4.4.1	Static Dissipation	188
4.4.2	Dynamic Dissipation	190
4.4.3	Low-power Design	191
4.5	Interconnect	196
4.5.1	Resistance	198
4.5.2	Capacitance	200
4.5.3	Delay	205
4.5.4	Crosstalk	207
 4.5.5	Inductance	210
 4.5.6	Temperature Dependence	216
 4.5.7	An Aside on Effective Resistance and Elmore Delay	216
4.6	Wire Engineering	219
4.6.1	Width and Spacing	219
4.6.2	Layer Selection	219
4.6.3	Shielding	221
4.6.4	Repeaters	221
4.6.5	Implications for Logical Effort	227
 4.6.6	Crosstalk Control	227
 4.6.7	Low-swing Signaling	229
4.7	Design Margin	231
4.7.1	Supply Voltage	232
4.7.2	Temperature	232
4.7.3	Process Variation	233

4.7.4	Design Corners	233
4.7.5	Matching	235
4.7.6	Delay Tracking	237
4.8	Reliability	239
4.8.1	Reliability Terminology	239
4.8.2	Electromigration	240
4.8.3	Self-heating	241
4.8.4	Hot Carriers	241
4.8.5	Latchup	242
4.8.6	Overvoltage Failure	244
4.8.7	Soft Errors	245
4.9	Scaling	245
4.9.1	Transistor Scaling	246
4.9.2	Interconnect Scaling	249
4.9.3	International Technology Roadmap for Semiconductors	251
4.9.4	Impacts on Design	252
4.10	Pitfalls and Fallacies	258
4.11	Historical Perspective	259
	Summary	264
	Exercises	266

CHAPTER 5 Circuit Simulation

5.1	Introduction	273
5.2	A SPICE Tutorial	274
5.2.1	Sources and Passive Components	274
5.2.2	Transistor DC Analysis	279
5.2.3	Inverter Transient Analysis	280
5.2.4	Subcircuits and Measurement	281
5.2.5	Optimization	284
5.2.6	Other HSPICE Commands	286
5.3	Device Models	287
5.3.1	Level 1 Models	287
5.3.2	Level 2 and 3 Models	288
5.3.3	BSIM Models	288
5.3.4	Diffusion Capacitance Models	289
5.3.5	Design Corners	290
5.4	Device Characterization	292
5.4.1	I-V Characteristics	293
5.4.2	Threshold Voltage	293
5.4.3	Gate Capacitance	296

5.4.4	Parasitic Capacitance	299
5.4.5	Effective Resistance	299
5.4.6	Comparison of Processes	301
5.4.7	Process and Environmental Sensitivity	303
5.5	Circuit Characterization	303
5.5.1	Path Simulations	305
5.5.2	DC Transfer Characteristics	305
5.5.3	Logical Effort	306
5.5.4	Power and Energy	309
5.5.5	Simulating Mismatches	310
5.5.6	Monte Carlo Simulation	310
5.6	Interconnect Simulation	311
5.7	Pitfalls and Fallacies	315
	Summary	316
	Exercises	317

CHAPTER 6 **Combinational Circuit Design**

6.1	Introduction	319
6.2	Circuit Families	320
6.2.1	Static CMOS	321
6.2.2	Ratioed Circuits	327
6.2.3	Cascode Voltage Switch Logic	331
6.2.4	Dynamic Circuits	332
6.2.5	Pass-transistor Circuits	345
6.3	Circuit Pitfalls	350
6.3.1	Threshold Drops	351
6.3.2	Ratio Failures	352
6.3.3	Leakage	352
6.3.4	Charge Sharing	353
6.3.5	Power Supply Noise	353
6.3.6	Hot Spots	354
6.3.7	Minority Carrier Injection	355
6.3.8	Back-gate Coupling	356
6.3.9	Diffusion Input Noise Sensitivity	357
6.3.10	Process Sensitivity	357
6.3.11	Example: Domino Noise Budgets	357
6.4	More Circuit Families	359
6.4.1	Differential Circuits	359
6.4.2	Sense-amplifier Circuits	360

6.4.3	BiCMOS Circuits	365
6.4.4	Other Circuit Families	365
6.5	Low-power Logic Design	366
6.6	Comparison of Circuit Families	367
6.7	Silicon-on-Insulator Circuit Design	369
6.7.1	Floating Body Voltage	370
6.7.2	SOI Advantages	371
6.7.3	SOI Disadvantages	372
6.7.4	Implications for Circuit Styles	373
6.7.5	Summary	373
6.8	Pitfalls and Fallacies	374
6.9	Historical Perspective	375
	Summary	377
	Exercises	378

CHAPTER 7 Sequential Circuit Design

7.1	Introduction	383
7.2	Sequencing Static Circuits	384
7.2.1	Sequencing Methods	385
7.2.2	Max-Delay Constraints	388
7.2.3	Min-delay Constraints	392
7.2.4	Time Borrowing	396
7.2.5	Clock Skew	399
7.3	Circuit Design of Latches and Flip-flops	402
7.3.1	Conventional CMOS Latches	402
7.3.2	Conventional CMOS Flip-flops	405
7.3.3	Pulsed Latches	407
7.3.4	Resettable Latches and Flip-flops	408
7.3.5	Enabled Latches and Flip-flops	410
7.3.6	Incorporating Logic into Latches	410
7.3.7	Klass Semidynamic Flip-flop (SDFF)	411
7.3.8	Differential Flip-flops	412
7.3.9	True Single-phase-clock (TSPC) Latches and Flip-flops	414
7.4	Static Sequencing Element Methodology	414
7.4.1	Choice of Elements	415
7.4.2	Low-power Sequential Design	417
7.4.3	Two-phase Timing Types	418
7.4.4	Characterizing Sequencing Element Delays	422

	7.5 Sequencing Dynamic Circuits	426
	7.5.1 Traditional Domino Circuits	427
	7.5.2 Skew-tolerant Domino Circuits	428
	7.5.3 Unfooted Domino Gate Timing	438
	7.5.4 Nonmonotonic Techniques	441
	7.5.5 Static-to-domino Interface	449
	7.5.6 Delayed Keepers	453
	7.6 Synchronizers	453
	7.6.1 Metastability	454
	7.6.2 A Simple Synchronizer	458
	7.6.3 Communicating Between Asynchronous Clock Domains	460
	7.6.4 Common Synchronizer Mistakes	461
	7.6.5 Arbiters	463
	7.6.6 Degrees of Synchrony	464
	7.7 Wave Pipelining	464
	7.8 Pitfalls and Fallacies	467
	7.9 Case Study: Pentium 4 and Itanium 2	
	Sequencing Methodologies	468
	7.9.1 Pentium 4 Sequencing	470
	7.9.2 Itanium 2 Sequencing	470
	Summary	473
	Exercises	475

CHAPTER 8 Design Methodology and Tools

8.1 Introduction	479
8.2 Structured Design Strategies	481
8.2.1 A Software Radio—A System Example	482
8.2.2 Hierarchy	485
8.2.3 Regularity	488
8.2.4 Modularity	492
8.2.5 Locality	495
8.2.6 Summary	498
8.3 Design Methods	498
8.3.1 Microprocessor/DSP	498
8.3.2 Programmable Logic	499
8.3.3 Gate Array and Sea of Gates Design	507
8.3.4 Cell-based Design	509
8.3.5 Full Custom Design	511
8.3.6 Platform-based Design—System on a Chip	518
8.3.7 Summary	519

8.4	Design Flows	520
8.4.1	Behavioral Synthesis Design Flow (ASIC Design Flow)	522
8.4.2	Automated Layout Generation	528
8.4.3	Mixed-signal or Custom-design Flow	532
8.4.4	Programmed Behavioral Synthesis	535
8.5	Design Economics	535
8.5.1	Non-recurring Engineering Costs (NREs)	537
8.5.2	Recurring Costs	539
8.5.3	Fixed Costs	541
8.5.4	Schedule	541
8.5.5	Personpower	542
8.5.6	Project Management	544
8.5.7	Design Reuse	544
8.6	Data Sheets and Documentation	545
8.6.1	The Summary	545
8.6.2	Pinout	546
8.6.3	Description of Operation	546
8.6.4	DC Specifications	546
8.6.5	AC Specifications	546
8.6.6	Package Diagram	547
8.6.7	Principles of Operation Manual	547
8.6.8	User Manual	547
 8.7	Closing the Gap between ASIC and Custom	547
8.7.1	Microarchitecture	548
8.7.2	Sequencing Overhead	548
8.7.3	Circuit Families	549
8.7.4	Logic Design	549
8.7.5	Cell and Wire Design	550
8.7.6	Layout	550
8.7.7	Process Variation	550
8.7.8	Summary	551
8.8	CMOS Physical Design Styles	551
8.8.1	Static CMOS Gate Layout	551
8.8.2	General CMOS Layout Guidelines	553
8.8.3	Layout Optimization for Performance	556
8.9	Interchange Formats	558
8.9.1	GDS2 Stream	558
8.9.2	Caltech Intermediate Format (CIF)	558
8.9.3	Library Exchange Format (LEF)	558
8.9.4	Design Exchange Format (DEF)	559
8.9.5	Standard Delay Format (SDF)	560
8.9.6	DSPF and SPEF	561

8.9.7	Advanced Library Format (ALF)	562
8.9.8	WAVES Waveform and Vector Exchange Specification	562
8.9.9	Physical Design Exchange Format (PDEF)	563
8.9.10	OpenAccess	563
8.10	Historical Perspective	564
8.11	Pitfalls and Fallacies	564
	Exercises	565

CHAPTER 9 Testing and Verification

9.1	Introduction	567
9.1.1	Logic Verification	568
9.1.2	Basic Digital Debugging Hints	570
9.1.3	Manufacturing Tests	573
9.2	Testers, Test Fixtures, and Test Programs	575
9.2.1	Testers and Test Fixtures	575
9.2.2	Test Programs	577
9.2.3	Handlers	579
9.3	Logic Verification Principles	579
9.3.1	Test Benches and Harnesses	579
9.3.2	Regression Testing	582
9.3.3	Version Control	584
9.3.4	Bug Tracking	584
9.4	Silicon Debug Principles	584
9.5	Manufacturing Test Principles	588
9.5.1	Fault Models	589
9.5.2	Observability	592
9.5.3	Controllability	592
9.5.4	Fault Coverage	593
9.5.5	Automatic Test Pattern Generation (ATPG)	593
9.5.6	Delay Fault Testing	594
9.6	Design for Testability	594
9.6.1	<i>Ad hoc</i> testing	595
9.6.2	Scan Design	596
9.6.3	Built-in Self-Test (BIST)	602
9.6.4	IDDQ Testing	608
9.6.5	Design for Manufacturability	608
9.7	Boundary Scan	609
9.7.1	The Test Access Port (TAP)	611
9.7.2	The Test Logic Architecture and Test Access Port	611

9.7.3	The TAP Controller	612
9.7.4	The Instruction Register	614
9.7.5	Test Data Registers	616
9.7.6	Summary	620
9.8	System-on-chip (SOC) Testing	622
9.9	Mixed-signal Testing	625
9.10	Reliability Testing	626
9.11	Testing in a University Environment	627
9.12	Pitfalls and Fallacies	629
	Summary	635
	Exercises	636

CHAPTER 10 Datapath Subsystems

10.1	Introduction	637
10.2	Addition/Subtraction	638
10.2.1	Single-bit Addition	638
10.2.2	Carry-propagate Addition	645
10.2.3	Adder Variants	677
10.3	One/Zero Detectors	679
10.4	Comparators	681
10.4.1	Magnitude Comparator	681
10.4.2	Equality Comparator	681
10.4.3	$K = A + B$ Comparator	682
10.5	Counters	683
10.5.1	Binary Counters	683
10.5.2	Linear-feedback Shift Registers	684
10.6	Boolean Logical Operations	686
10.7	Coding	686
10.7.1	Parity	687
10.7.2	Error-correcting Codes	687
10.7.3	Gray Codes	688
10.7.4	XOR/XNOR Circuit Forms	689
10.8	Shifters	691
10.9	Multiplication	693
10.9.1	Unsigned Array Multiplication	694
10.9.2	2's Complement Array Multiplication	696
10.9.3	Booth Encoding	698

	10.9.4	Wallace Tree Multiplication	703
	10.9.5	Hybrid Multiplication	705
	10.9.6	Fused Multiply-Add	705
	10.9.7	Serial Multiplication	705
	10.10	Parallel-prefix Computations	706
	10.11	Pitfalls and Fallacies	708
	10.12	Historical Perspective	709
		Summary	709
		Exercises	710

CHAPTER 11 Array Subsystems

	11.1	Introduction	713
	11.2	SRAM	715
	11.2.1	Memory Cell Read/Write Operation	718
	11.2.2	Decoders	719
	11.2.3	Bitline Conditioning and Column Circuitry	725
	11.2.4	Multi-ported SRAM and Register Files	728
	11.2.5	Large SRAMs	730
	11.2.6	Logical Effort of RAMs and Register Files	731
	11.2.7	Case Study: Itanium 2 Cache	733
	11.3	DRAM	734
	11.3.1	Subarray Architectures	735
	11.3.2	Column Circuitry	738
	11.3.3	Applications to CMOS Systems-on-chip	738
	11.4	Read-only Memory	739
	11.4.1	Programmable ROMs	741
	11.4.2	NAND ROMs	743
	11.5	Serial Access Memories	744
	11.5.1	Shift Registers	745
	11.5.2	Queues (FIFO, LIFO)	746
	11.6	Content-addressable Memory	747
	11.7	Programmable Logic Arrays	750
	11.8	Array Yield, Reliability, and Self-test	756
	11.9	Historical Perspective	757
		Summary	759
		Exercises	760

CHAPTER 12 Special-purpose Subsystems

12.1	Introduction	761
12.2	Packaging	761
12.2.1	Package Options	762
12.2.2	Chip-to-package Connections	764
12.2.3	Package Parasitics	765
12.2.4	Heat Dissipation	765
12.3	Power Distribution	767
12.3.1	On-chip Power Distribution Network	768
12.3.2	IR Drops	771
12.3.3	$L di/dt$ Noise	772
12.3.4	On-chip Bypass Capacitance	773
 12.3.5	Power Network Modeling	775
 12.3.6	Signal Return Paths	778
 12.3.7	Power Supply Filtering	779
 12.3.8	Substrate Noise	780
12.4	I/O	780
12.4.1	Basic I/O Pad Circuits	781
12.4.2	Example: MOSIS I/O Pads	784
 12.4.3	Level Converters	784
12.5	Clock	786
12.5.1	Definitions	786
12.5.2	Clock System Architecture	789
12.5.3	Global Clock Generation	790
12.5.4	Global Clock Distribution	793
12.5.5	Local Clock Gaters	798
 12.5.6	Clock Skew Budgets	800
 12.5.7	Adaptive Deskewing	806
 12.5.8	Clocking Alternatives	807
12.6	Analog Circuits	808
12.6.1	MOS Small-signal Model	808
12.6.2	Common Source Amplifier	811
12.6.3	The CMOS Inverter as an Amplifier	812
12.6.4	Current Mirrors	814
12.6.5	Differential Pairs	816
12.6.6	Simple CMOS Operational Amplifier	819
12.6.7	Digital-to-analog and Analog-to-digital Converter Basics	819
12.6.8	Digital-to-analog Converters	824
12.6.9	Analog-to-digital Converters	828
12.6.10	Radio Frequency (RF) Circuits	837
12.6.11	Analog Summary	841

12.7	Pitfalls and Fallacies	842
12.8	Historical Perspective	843
	Summary	845
	Exercises	845
APPENDIX A	Verilog	
A.1	Introduction	849
A.2	Behavioral Modeling with Continuous Assignments	850
	A.2.1 Bitwise Operators	850
	A.2.2 Comments and White Space	851
	A.2.3 Reduction Operators	851
	A.2.4 Other Operators	852
A.3	Basic Constructs	852
	A.3.1 Internal Signals	852
	A.3.2 Precedence	853
	A.3.3 Constants	854
	A.3.4 Hierarchy	854
	A.3.5 Tristates	855
	A.3.6 Bit Swizzling	855
	A.3.7 Delays	857
A.4	Behavioral Modeling with Always Blocks	857
	A.4.1 Registers	857
	A.4.2 Latches	859
	A.4.3 Counters	859
	A.4.4 Combinational Logic	860
	A.4.5 Memories	866
	A.4.6 Blocking and Nonblocking Assignment	867
A.5	Finite State Machines	868
A.6	Parameterized Modules	874
A.7	Structural Primitives	874
A.8	Test Benches	875
A.9	Pitfalls	877
	A.9.1 Verilog Style Guidelines	877
	A.9.2 Incorrect Stimulus List	878
	A.9.3 Missing begin/end Block	880
	A.9.4 Undefined Outputs	880
	A.9.5 Incomplete Specification of Cases	882

A.9.6	Shorted Outputs	884
A.9.7	Incorrect Use of Nonblocking Assignments	885
A.10	Example: MIPS Processor	886

APPENDIX B VHDL

B.1	Introduction	895
B.2	Behavioral Modeling with Concurrent Signal Assignments	896
B.2.1	Bitwise Operators	896
B.2.2	Comments and White Space	897
B.2.3	Other Operators	897
B.2.4	Conditional Signal Assignment Statements	898
B.2.5	Selected Signal Assignment Statements	898
B.3	Basic Constructs	899
B.3.1	Blocks, Entities, and Architectures	899
B.3.2	Internal Signals	900
B.3.3	Precedence	900
B.3.4	Hierarchy	901
B.3.5	Bit Swizzling	901
B.3.6	Types	902
B.3.7	Library and Use Clauses	904
B.3.8	Tristates	905
B.3.9	Delays	906
B.4	Behavioral Modeling with Process Statements	906
B.4.1	Flip-flops	906
B.4.2	Latches	908
B.4.3	Counters	908
B.4.4	Combinational Logic	909
B.4.5	Memories	912
B.5	Finite State Machines	913
B.6	Parameterized Blocks	915
B.7	Example: MIPS Processor	917

References 927

Index 953