

Table of Contents

Power-Aware Microarchitectural/Circuit Techniques

System-Level Design Methods for Low-Energy Architectures Containing Variable Voltage Processors	1
<i>F. Gruian (Lund University)</i>	
Ramp Up/Down Functional Unit to Reduce Step Power	13
<i>Z. Tang (University of Wisconsin), N. Chang, S. Lin, W. Xie, S. Nakagawa (HP Labs), and L. He (University of Wisconsin)</i>	
An Adaptive Issue Queue for Reduced Power at High Performance	25
<i>A. Buyuktosunoglu (University of Rochester), S. Schuster (IBM Watson), D. Brooks (Princeton University/IBM Watson), P. Bose, P. Cook (IBM Watson), and D. Albonesi (University of Rochester)</i>	

Application/Compiler Optimizations

Dynamic Memory Oriented Transformations in the MPEG4 IM1-Player on a Low Power Platform	40
<i>P. Marchal, C. Wong (IMEC/K.U. Leuven-ESAT), A. Prayati (University of Patras), N. Cossement (K.U. Leuven-ESAT), F. Catthoor (IMEC/K.U. Leuven-ESAT), R. Lauwereins (K.U. Leuven-ESAT), D. Verkest (IMEC), and H. De Man (IMEC/K.U. Leuven-ESAT)</i>	
Exploiting Content Variation and Perception in Power-Aware 3D Graphics Rendering	51
<i>J. Euh and W. Burleson (University of Massachusetts)</i>	
Compiler-Directed Dynamic Frequency and Voltage Scheduling	65
<i>C.-H. Hsu, U. Kremer, and M. Hsiao (Rutgers University)</i>	

Exploiting IPC/Memory Slack

Cache-Line Decay: A Mechanism to Reduce Cache Leakage Power	82
<i>S. Kaxiras (Lucent Technologies), Z. Hu (Princeton University), G. Narlikar, and R. McLellan (Lucent Technologies)</i>	
Dynamically Reconfiguring Processor Resources to Reduce Power Consumption in High-Performance Processors	97
<i>R. Maro (Brown University/Politecnico di Torino), Y. Bai, and R.I. Bahar (Brown University)</i>	

Power/Performance Models and Tools

TEM²P²EST: A Thermal Enabled Multi-model Power/Performance
ESTimator 112
 *A. Dhodapkar (University of Wisconsin), C.H. Lim (Intel/Portland
 State University), G. Cai (Intel), and W.R. Daasch (Portland State
 University)*

Power-Performance Modeling and Tradeoff Analysis for
a High End Microprocessor 126
 *D. Brooks (Princeton University), M. Martonosi (Princeton
 University), J.-D. Wellman, and P. Bose (IBM Watson)*

A Comparison of Two Architectural Power Models 137
 S. Ghiasi and D. Grunwald (University of Colorado)

Author Index 153