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Modern design of complex systems, especially electronic ones, requires that their behavior have to be (and mostly are) formalized. Formalization and automation of system design requires developing of formal models for parallel discrete devices and low-level description languages based on these models.

Formalizations of devices and systems described in VHDL, Verilog or other assembly languages of logical control, as LD, E- or NF [159], are very difficult for formal verification, because it is practically impossible to create adequate and at the same time simple formal models for such specifications (if these languages are used without restrictions). The problem can be solved by using restricted specifications based on models which are easy to analyze and have enough expressive power.

There are two main directions of developing such models, each having its pros and cons aspects. Both of them are, in a sense, extensions of the finite state machine (FSM) – the basic model of sequential discrete devices, which is, of course, in its “pure” version not convenient for practical needs of specifying of complex systems.

The first direction is the composition of FSMs in various ways. The simplest and most generalization of this approach is the FSM network – a system of communicating automata [22, 147]. Studies on the automata networks have started in 1960-ies. The typical development of the methods of behavior specification by means of such automata began in 1980-ies. Adding hierarchy to FSM networks leads to obtaining the model known as HCPSM (Hierarchical Concurrent Finite State Machines) [23]. One of the most popular and well-adapted to HCPSM languages has been developed within a frame of the universal specification language UML (Unified Modeling Language [209]), describing hierarchical objects and dependencies between them. We talk about the Statecharts, invented by D. Harel [56, 62]. There are several other models and languages based on automata networks such as